***CSE 577 – Phase 1, Part 2***

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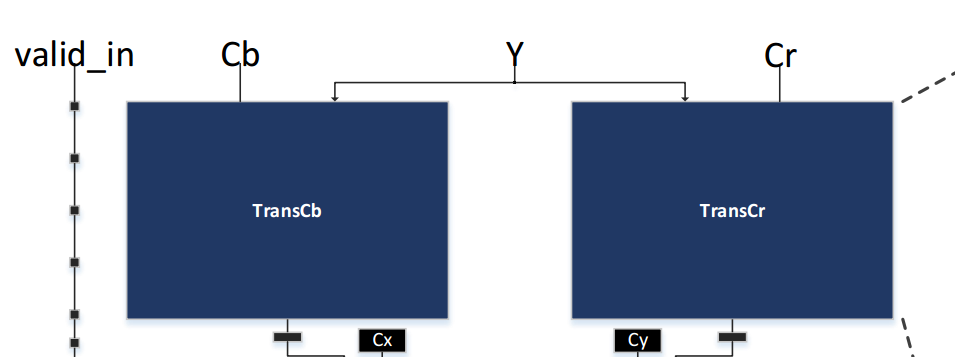
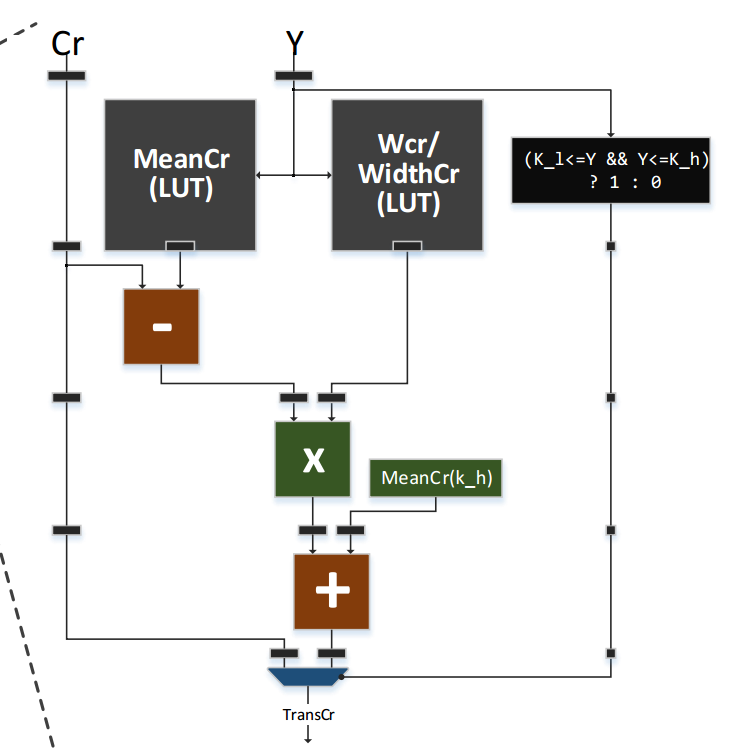
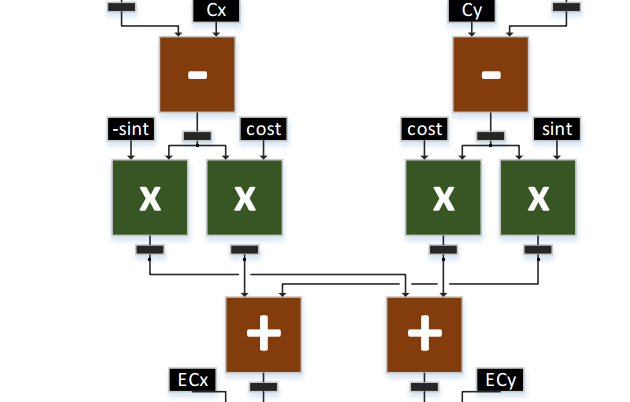
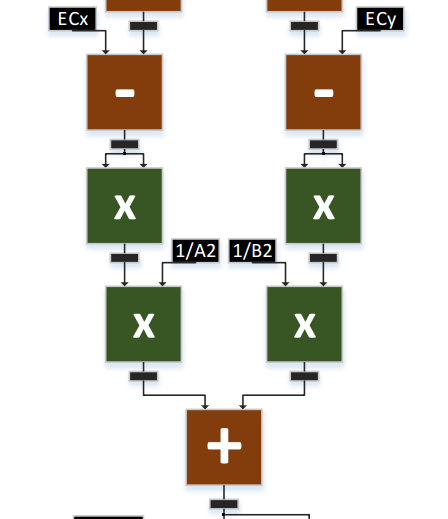
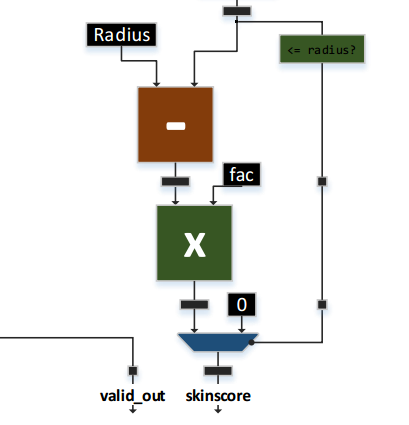
# Purpose

The purpose of this part of the project is to design the Verilog code that meet that the specification.

# Design

## Breaking Flow Diagram into chunks

In order to make the Verilog code more manageable, the design flow diagram was broken into chunks. Each of these chunks are then converted into a Verilog module. The final Verilog code is composed of mainly 4 stages. These stages are:

1. Stage 1
   1. Stage 1 is composed of the following blocks
      1. 
      2. 
2. Stage 2
   1. Stage 2 is composed of these blocks
      1. 
3. Stage 3
   1. Stage 3 is composed of the following blocks
      1. 
4. Stage 4
   1. Stage 4 is composed of the following blocks
      1. 

## Verilog files layout

Each of the Verilog files were emulate the stages specified above.

* Stage 1 is composed of transcb.v and transcr.v files
  + transcb.v output signal = cb\_stage2
  + transcr.v output signal = cr\_stage2
* Stage 2 is composed of stage2.v
  + stage2.v output signals = st2\_st3\_1 and st2\_st3\_2
* Stage 3 is composed of stage3.v
  + stage3.v output signals = st3\_st4
* Stage 4 is composed of stage4.v
  + stage4.v output signal = skinScore

skintoneDetector.v acts as the top module and form the complete program.

## Data representation

Calculations in the design were done using 32 bits Q.14 fixed point representation, meaning 14 of the 32 bits were dedicated to the fractional part.

Below is the table of the output signals from the stages their respective data representation.

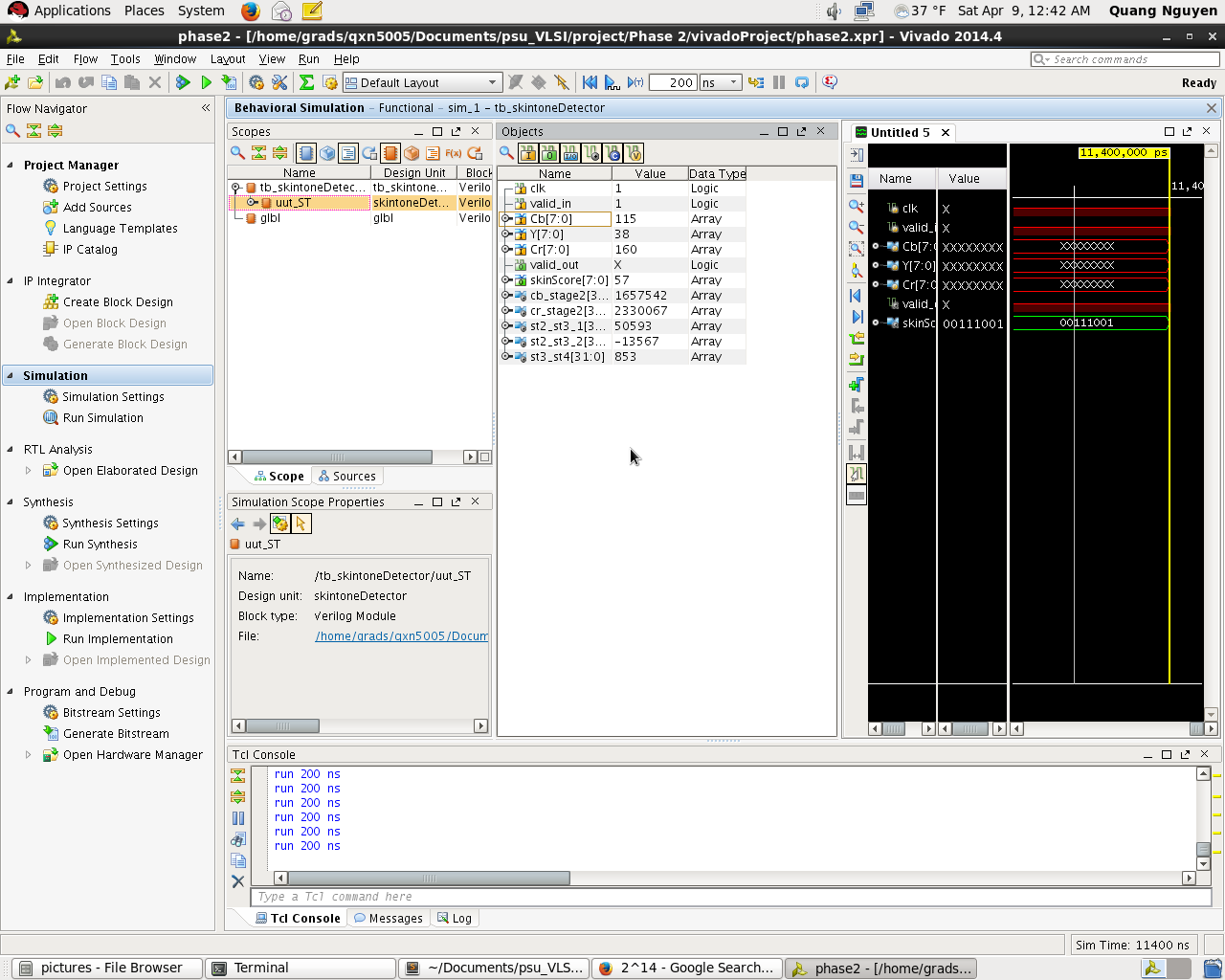
|  |  |
| --- | --- |
| cb\_stage2 | 32 bit, Q.14 |
| cr\_stage2 | 32 bit, Q.14 |
| st2\_st3\_1 | 32 bit, Q.14 |
| st2\_st3\_2 | 32 bit, Q.14 |
| st3\_st4 | 32 bit, Q.14 |
| skinScore | 8 bit |

# Testing and Verification

Each stages of the design was also calculated using python code. This repetitive calculation allows us to compare the output values of our design with the expected output values.

## Method

The design was simulated using Vivado simulator. The inputs were then drive using the “force constant” functionality of the simulator. The below is a picture depicting the signals that were driving the design’s outputs.



Different values of Y, Cr, and Cb were used and the design’s corresponding output signals were then recorded

## Results

Due to time constrains we were unable to get our design to yield the same values as the expected values. The tables below show our expected vs received values.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***Expected Output - Output from Python code*** | | | | | | | | |
| Y | Cr | Cb | cb\_stage2 | cr\_stage2 | st2\_st3\_1 | st2\_st3\_2 | st3\_st4 | skinScore |
| 120 | 96 | 160 | 2615985 | 1560455 | 117702 | 235572 | 187392 | 0 |
| 76 | 130 | 182 | 1926437 | 3247257 | -867421 | -1297498 | 9696059 | 0 |
| 76 | 130 | 201 | 1926437 | 3651229 | -1198167 | -1529448 | 14312298 | 0 |
| 76 | 132 | 182 | 1968317 | 3247257 | -891467 | -1263210 | 9407008 | 0 |
| 76 | 132 | 191 | 1968317 | 3438612 | -1048137 | -1373080 | 11455070 | 0 |
| 1 | 1 | 1 | -3469743 | -2854424 | 7226573 | -2212122 | 146685945 | 0 |
| 20 | 90 | 150 | 262926 | 2812545 | 443633 | -2409873 | 26518050 | 0 |
| 38 | 160 | 115 | 2470230 | 1742335 | 52480 | 11807 | 4991 | 99 |
| 112 | 153 | 109 | 2485010 | 1766110 | 24527 | 10257 | 3723 | 139 |
| 136 | 152 | 105 | 0 | 0 | 58942 | 40935 | 2583 | 102 |
| 190 | 156 | 106 | 2541134 | 1728508 | 23089 | 77797 | 6409 | 55 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***Received Output - Output from design*** | | | | | | | | |
| Y | Cr | Cb | cb\_stage2 | cr\_stage2 | st2\_st3\_1 | st2\_st3\_2 | st3\_st4 | skinScore |
| 120 | 96 | 160 | -571331 | 3383348 | 355615 | 521951 | 79541 | 0 |
| 76 | 130 | 182 | 12073708 | -1016494 | -1601039 | -2193676 | 1752694 | 0 |
| 76 | 130 | 201 | 14890505 | -1016494 | -2177585 | -2597998 | 2619487 | 0 |
| 76 | 132 | 182 | 12073708 | -768059 | -1636699 | -2142826 | 1709306 | 0 |
| 76 | 132 | 191 | 13407980 | -768059 | -1909800 | -2334347 | 2094007 | 0 |
| 1 | 1 | 1 | -7783095 | -9204359 | 3638561 | -1019345 | 2264274 | 0 |
| 20 | 90 | 150 | 4935312 | -3716506 | 247617 | -1721677 | 850132 | 0 |
| 38 | 160 | 115 | 1657542 | 2330067 | 50593 | -13567 | 853 | 57 |
| 112 | 153 | 109 | 1734668 | 2195127 | 54176 | -52257 | 2403 | 45 |
| 136 | 152 | 105 | 1720320 | 2473984 | 17086 | 6879 | 300 | 61 |
| 190 | 156 | 106 | 1316775 | 2686699 | 69151 | 108343 | 1564 | 51 |

# Summary

As stated in the section above, our design did not pass the verification step. Due to time constrains, we were unable to move further in debugging. As it stands, our design is pipelined and functional.